

FIG. 1

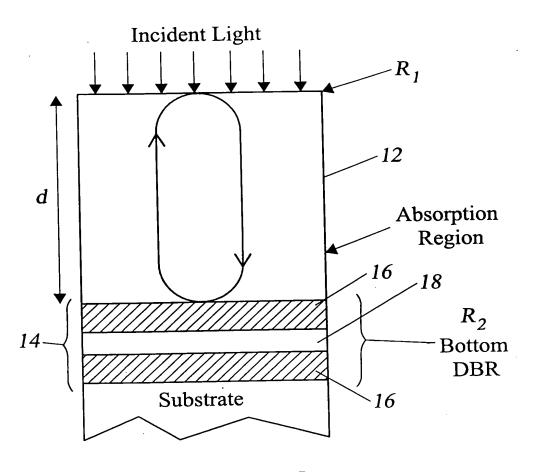
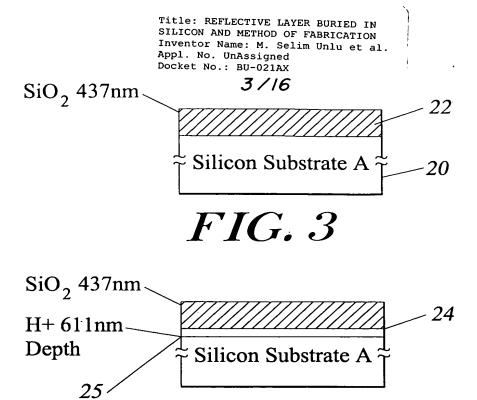


FIG. 2



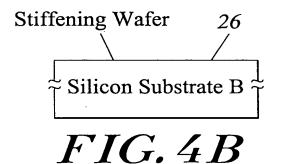
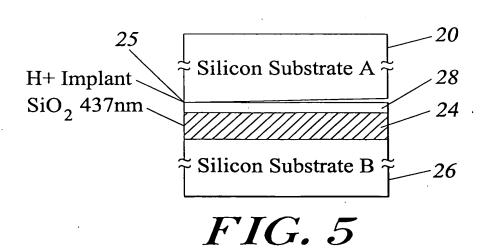
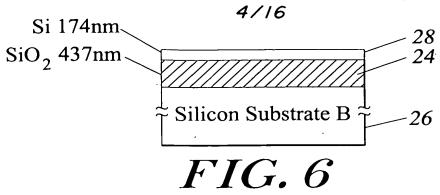
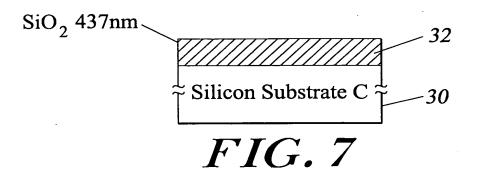


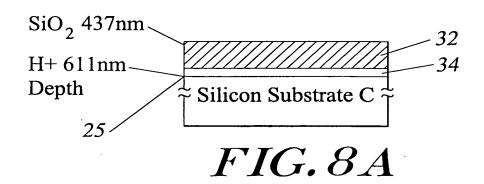
FIG. 4A

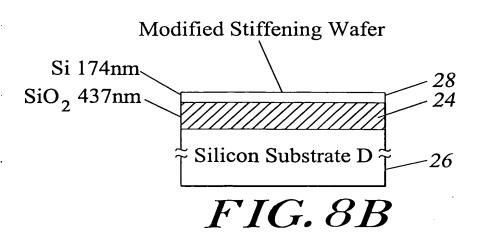


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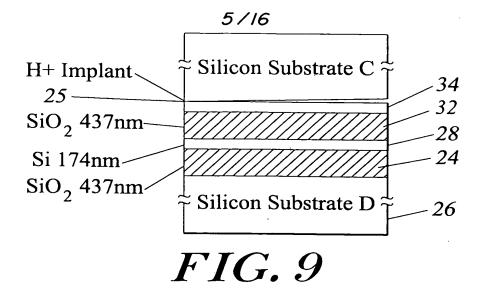


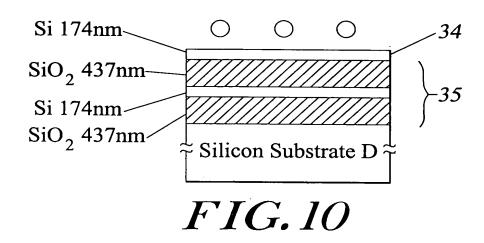


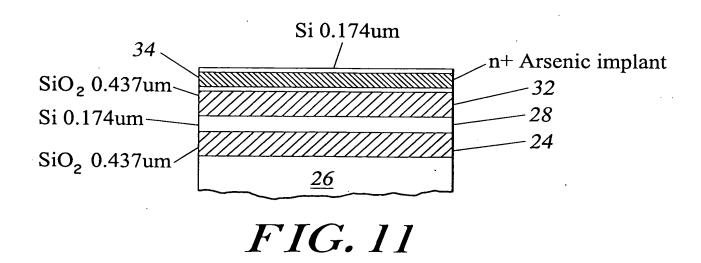


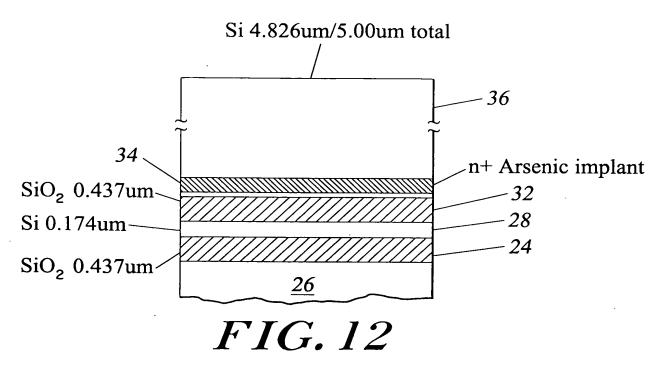


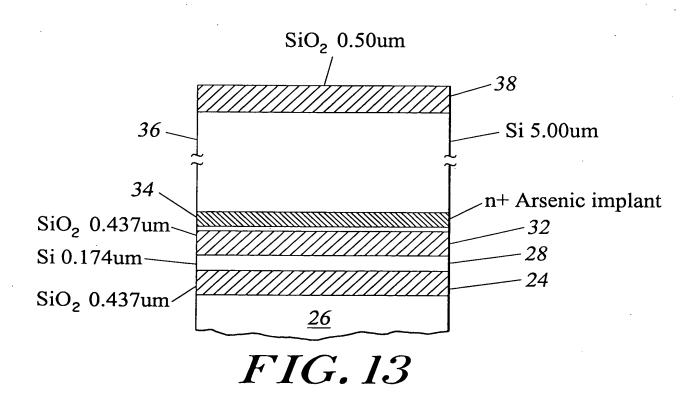
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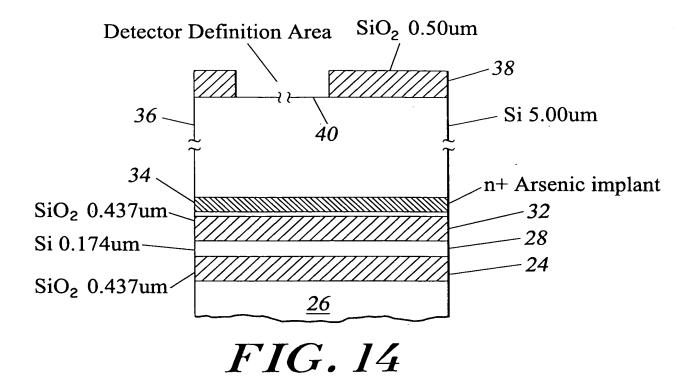


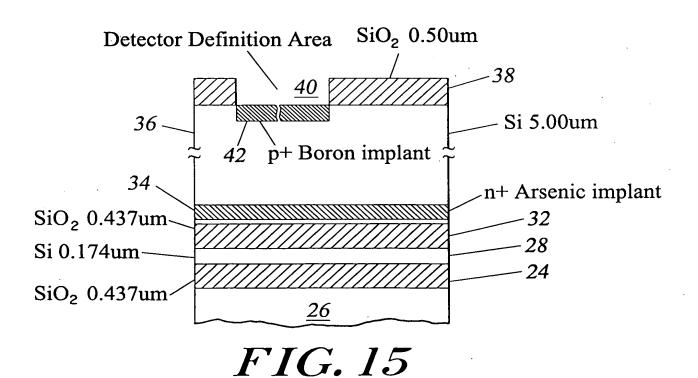


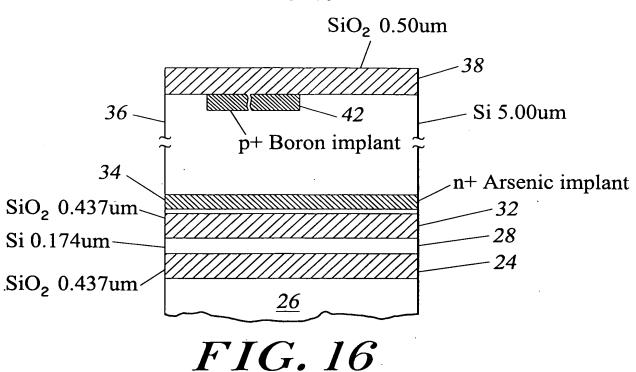


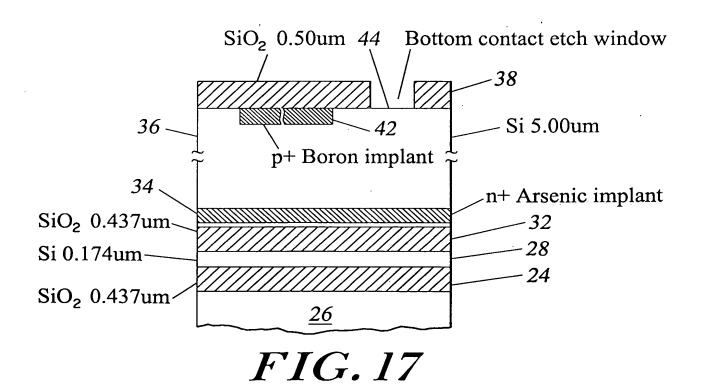


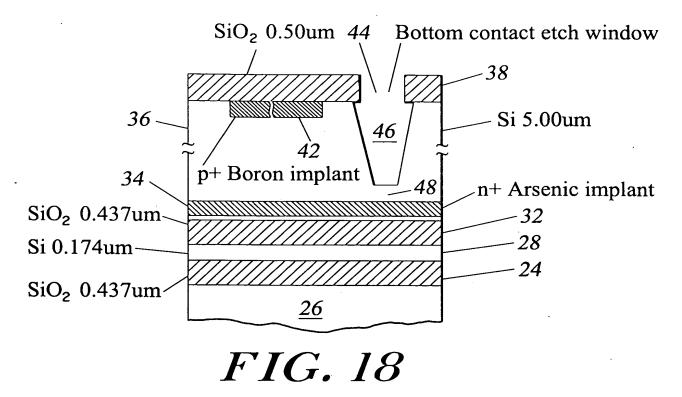


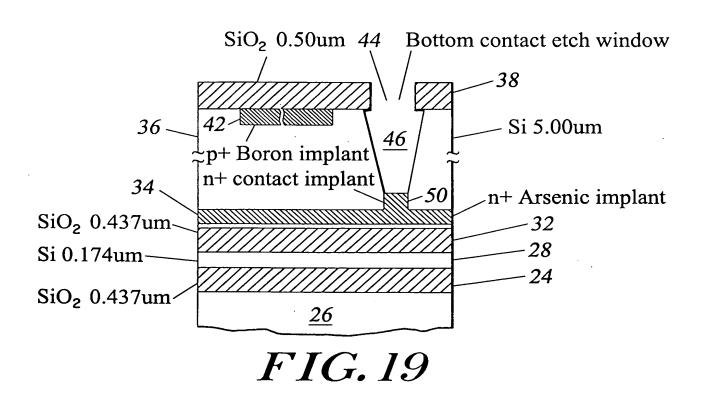


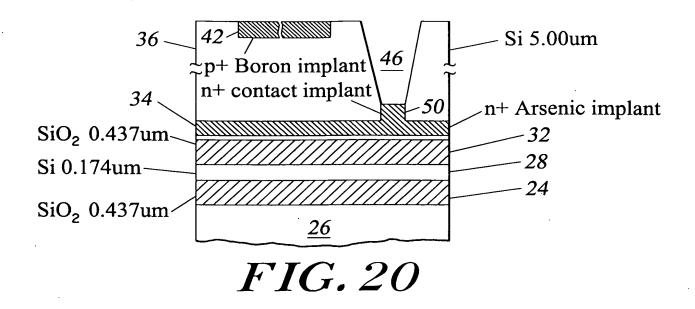


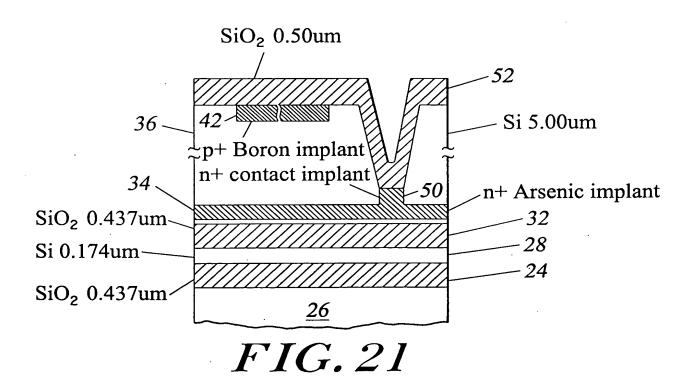


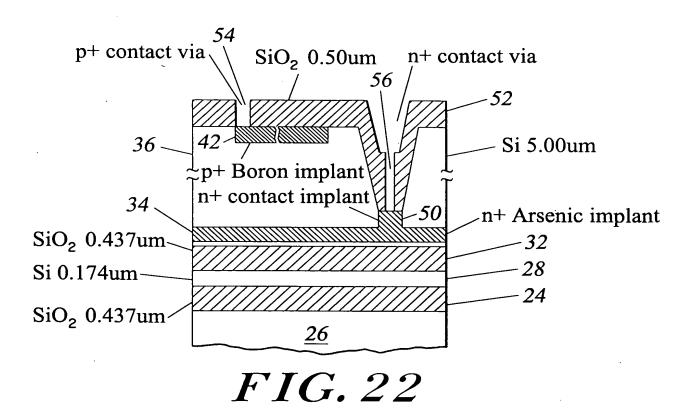


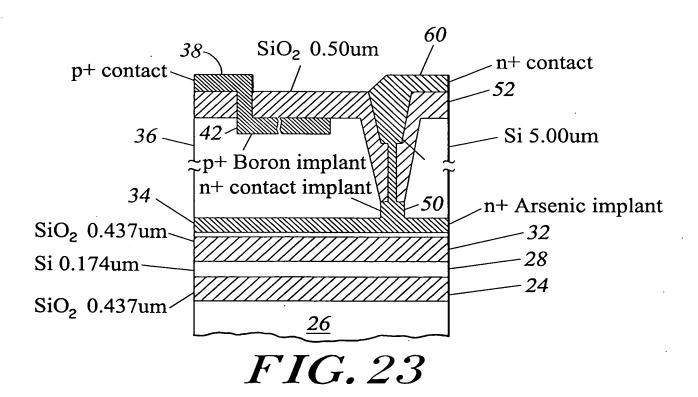




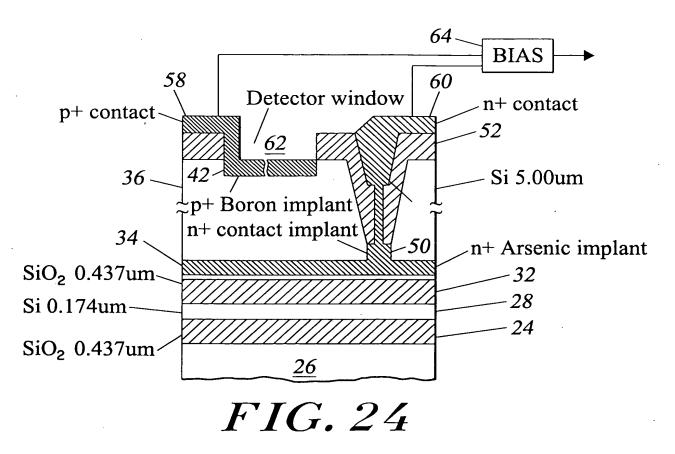


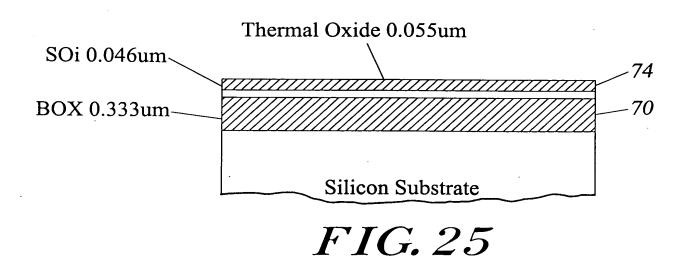




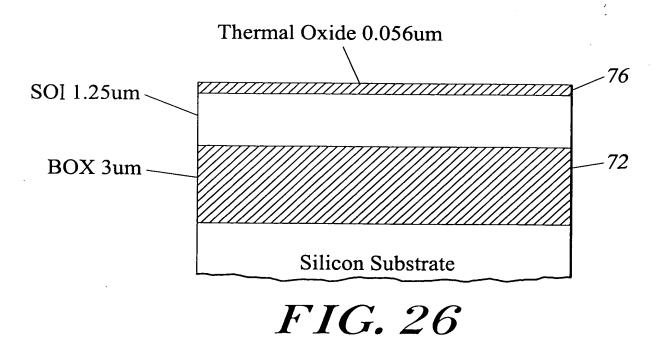


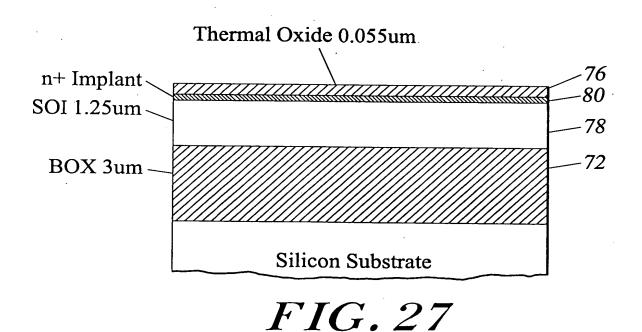
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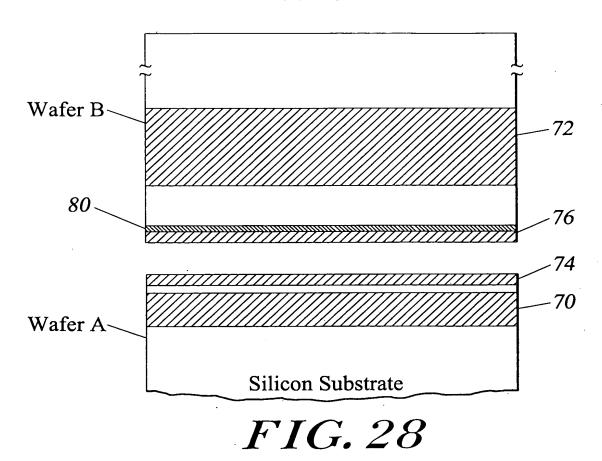


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Thin Silicon Layer

Top Oxide

Si 1.25um
n+ region
SiO₂ 0.111um
Si 0.046um
SiO₂ 0.333um

Silicon Substrate

FIG. 29

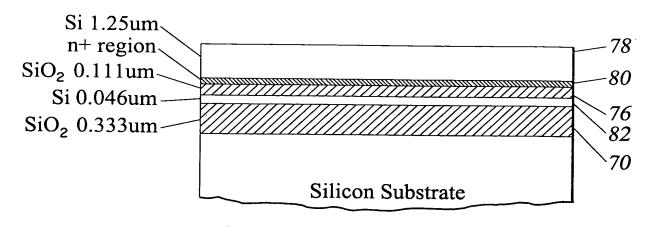


FIG. 30

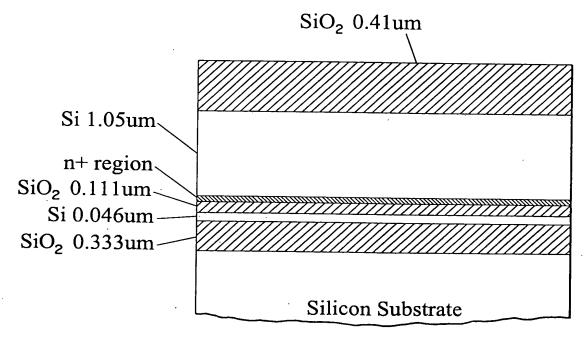


FIG. 31

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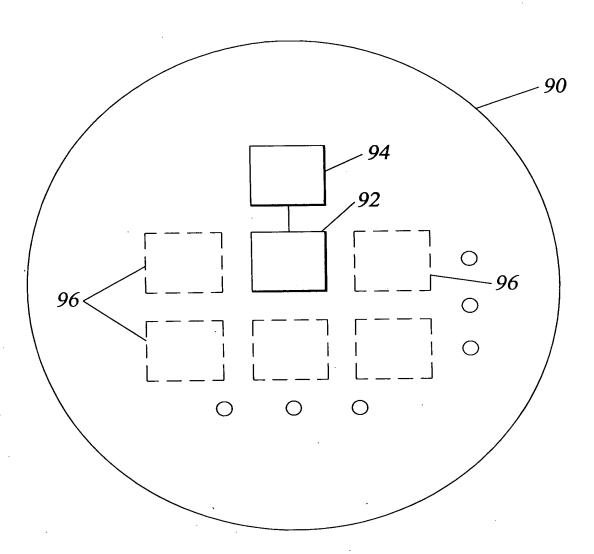


FIG. 32